Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L9	L5 and l7	3	L9
L8	l5 same first memory same second memory	2	L8
L7	first memory same second memory	23532	L7
L6	L5 same l3	3	L6
L5	L4 same l1	18	L5
L4	(multiple or plurality or more than one or numerous or various or first) adj3 data near2 width	764	L4
L3	(multiple or plurality or more than one or numerous or various or first) adj3 memory	111431	L3
L2	(multiple or plurality or more than one or numerous or various or first) adj3 data width	181	L2
L1	(multiple or plurality or more than one or numerous or various or first) adj3 data path	1915	L1

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☐ 1. Document ID: US 20020133682 A1

L5: Entry 1 of 18 File: PGPB Sep 19, 2002

DOCUMENT-IDENTIFIER: US 20020133682 A1
TITLE: System with wide operand architecture, and method

Detail Description Paragraph (8):
[0031] The execution functional units E 141, 149, execution functional units X-142, 148, and execution functional unit T each contain dedicated storage to permit storage of source operands including wide operands as discussed hereinafter. The dedicated storage 132-136, which may be thought of as a wide microcache, typically has a width which is a multiple of the width of the data path operands related to the data path source operand buses 151-158. Thus, if the width of the data path 151-158 is 128 bits, the dedicated storage 132-136 may have a width of 256, 512, 1024 or 2048 bits. Operands which utilize the full width of the dedicated storage are referred to herein as wide operands, although it is not necessary in all instances that a wide operand use the entirety of the width of the dedicated storage; it is sufficient that the wide operand use a portion greater than the width of the memory data path of the output of the memory system 117-120 and the functional unit data path of the input of the execution functional units 141-149, though not necessarily greater than the width of the two combined. Because the width of the dedicated storage 132-136 is greater than the width of the memory operand bus 137, portions of wide operands are loaded sequentially into the dedicated storage 132-136. However, once loaded, the wide operands may then be used at substantially the same time. It can be seen that functional units 141-149 and associated execution registers 125-128 form a data functional unit, the exact elements of which may vary with implementation.

Detail Description Paragraph (13):
[0036] The wide function unit may be better appreciated from FIG. 7, in which a register number 700 is provided to an operand checker 705. Wide operand specifier 710 communicates with the operand checker 705 and also addresses memory 715 having a defined memory width. The memory address includes a plurality of register operands 720A-n, which are accumulated in a dedicated storage portion 714 of a data functional unit 725. In the exemplary embodiment shown in FIG. 7, the dedicated storage 714 can be seen to have a width equal to eight data path widths, such that eight wide operand portions 730A-H are sequentially loaded into the dedicated storage to form the wide operand. Although eight portions are shown in FIG. 7, the present invention is not limited to eight or any other specific multiple of data path widths. Once the wide operand portions 730A-H are sequentially loaded, they may be used as a single wide operand 735 by the functional element 740, which may be any element(s) from FIG. 1 connected thereto. The result of the wide operand is then provided to a result register 745, which in a presently preferred embodiment is of the same width as the memory width.

Detail Description Paragraph (25):
[0048] Referring next to FIG. 9, an exemplary arrangement of the data structures of the wide microcache or dedicated storage114 may be better appreciated. The wide microcache contents, wmc.c, can be seen to form a plurality of data path widths 900A-n, although in the example shown the number is eight. The physical address, wmc.pa, is shown as 64 bits in the example shown, although the invention is not limited to a specific width. The size of the contents, wmc.size, is also provided in a field which is shown as 10 bits in an exemplary embodiment. A "contents valid" flag, wmc.cv, of one bit is also included in the data structure, together with a two bit field for thread last used, or wmc.th. In addition, a six bit field for register last used, wmc.reg, is provided in an exemplary embodiment. Further, a one bit flag for register and thread valid, or

wmc.rtv, may be provided.

CLAIMS:

1. In a system having a data path functional unit having a functional unit data path width, a first memory system having a first data path width, and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width, a method comprising: copying a first memory operand portion from the first memory system to the second memory system, the first memory operand portion having the first data path width; and copying a second memory operand portion from the first memory system to the second memory system, the second memory operand portion having the first data path width and being catenated in the second memory system with the first memory operand portion, thereby forming catenated data.

2. The method of claim 1 further comprising reading at least a portion of the catenated data which is greater in width than the first data path width.

3. The method of claim 2 further comprising specifying a memory specifier from which a plurality of data path widths of data can be read.

7. In a system having a data path functional unit having a functional unit data path width, a first memory system having a first data path width, and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width, a method comprising: copying a first memory operand portion from the first memory system to the second memory system, the first memory operand portion having the first data path width; copying a second memory operand portion from the first memory system to the second memory system, the second memory operand portion having the first data path width; and catenating the second memory operand portion in the second memory system with the first memory operand portion, thereby forming catenated data.

8. The method of claim 7 further comprising reading at least a portion of the catenated data which is greater in width than the first data path width.

9. The method of claim 8 further comprising specifying a memory specifier from which a plurality of data path widths of data can be read.

13. In a system having a data path functional unit having a functional unit data path width, a first memory system having a first data path width, and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width, a system comprising: a first copying module configured to copy a first memory operand portion from the first memory system to the second memory system, the first memory operand portion having the first data path width; and a second copying module configured to copy a second memory operand portion from the first memory system to the second memory system, the second memory operand portion having the first data path width and being catenated in the second memory system with the first memory operand portion, thereby forming catenated data.

14. The system of claim 13 further comprising a reading module configured to read at least a portion of the catenated data which is greater in width than the first data path width.

15. In a system having a data path functional unit having a functional unit data path width, a first memory system having a first data path width, and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width, a system comprising: a first copying module configured to copy a first memory operand portion from the first memory system to the second memory system, the first memory operand portion having the first data path width; and a second copying module configured to copy a second memory operand portion from the first memory system to the second memory system, the second memory operand portion having the first data path width.

17. The system of claim 16 further comprising a reading module configured to read at least a portion of the catenated data which is greater in width than the first data path width.

☐ 2. Document ID: US 20010001158 A1

L5: Entry 2 of 18 File: PGPB May 10, 2001

DOCUMENT-IDENTIFIER: US 20010001158 A1
TITLE: Memory array organization

CLAIMS:

19. A method of performing error correction in a memory, said method comprising: transferring data words of a predetermined width to and from a plurality of narrow data path memory devices through respective first narrow data path channels, a mutually exclusive group of the bits of the data words being transferred and stored in a respectively corresponding one of the plurality of first narrow data path memory devices in parallel with the other first narrow data path memory devices; transferring error correction data to a second narrow data path memory device through a respective second narrow data path channel; and detecting and correcting errors in the data stored in said plurality of first narrow data path memory devices using said error correction data stored in said second narrow data path memory device.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 6434674 B1

L5: Entry 3 of 18 File: USPT Aug 13, 2002

DOCUMENT-IDENTIFIER: US 6434674 B1
TITLE: Multiport memory architecture with direct data flow

CLAIMS:

1. A high-speed, multiport memory architecture for use with a processor, comprising: a) a first interface adapted for bi-directional connection to a first external data bus said first external data bus having a first data path width and a first data bus speed, said bi-directional connection being made through a first I/O port, said first interface having a second, bi-directional I/O port configured for bi-directional communication with a first internal data bus, and said first interface comprising a data sourcing controller; b) a second interface adapted for bi-directional connection to a second external data bus, said second external data bus having a second data path width and a second data bus speed, said bi-directional connection being made through a first I/O port, said second interface having a second, bi-directional I/O port configured for bi-directional communication with a second internal data bus, said second interface comprising a data consuming controller; c) a first plurality of bi-directional FIFO buffers each having a first buffer I/O port operatively connected to a first internal data bus and a second buffer I/O port configured for connection to a multiplexer; d) a second plurality of bi-directional FIFO buffers each having a first buffer I/O port operatively connected to a second internal data bus and a second buffer I/O port configured for connection to a multiplexer; e) a multiplexer having a plurality of inputs, each being connected to respective bi-directional FIFO buffers of said first and second plurality of bi-directional FIFO buffers; f) a memory operatively connected to said multiplexer, said memory having a data path width greater than said data path widths of said first external data bus and said second external data bus and a speed greater than said bus speed of said first external data bus and said external

data bus;

whereby data on said first external data bus is transferred to said second external data bus through: said first interface, said first internal data bus, at least one of said first plurality of bi-directional FIFO buffers, said memory, at least one of said second plurality of bi-directional FIFO buffers, said second internal data bus and said second interface.

☐ 4. Document ID: US 6295599 B1

L5: Entry 4 of 18 File: USPT Sep 25, 2001

DOCUMENT-IDENTIFIER: US 6295599 B1
TITLE: System and method for providing a wide operand architecture

Detailed Description Text (8):
The execution functional units E 141, 149, execution functional units X--142, 148, and execution functional unit T each contain dedicated storage to permit storage of source operands including wide operands as discussed hereinafter. The dedicated storage 132-136, which may be thought of as a wide microcache, typically has a width which is a multiple of the width of the data path operands related to the data path source operand buses 151-158. Thus, if the width of the data path 151-158 is 128 bits, the dedicated storage 132-136 may have a width of 256, 512, 1024 or 2048 bits. Operands which utilize the full width of the dedicated storage are referred to herein as wide operands, although it is not necessary in all instances that a wide operand use the entirety of the width of the dedicated storage; it is sufficient that the wide operand use a portion greater than the width of the memory data path of the output of the memory system 117-120 and the functional unit data path of the input of the execution functional units 141-149, though not necessarily greater than the width of the two combined. Because the width of the dedicated storage 132-136 is greater than the width of the memory operand bus 137, portions of wide operands are loaded sequentially into the dedicated storage 132-136. However, once loaded, the wide operands may then be used at substantially the same time. It can be seen that functional units 141-149 and associated execution registers 125-128 form a data functional unit, the exact elements of which may vary with implementation.

Detailed Description Text (13):
The wide function unit may be better appreciated from FIG. 7, in which a register number 700 is provided to an operand checker 705. Wide operand specifier 710 communicates with the operand checker 705 and also addresses memory 715 having a defined memory width. The memory address includes a plurality of register operands 720A-n, which are accumulated in a dedicated storage portion 714 of a data functional unit 725. In the exemplary embodiment shown in FIG. 7, the dedicated storage 714 can be seen to have a width equal to eight data path widths, such that eight wide operand portions 730A-H are sequentially loaded into the dedicated storage to form the wide operand. Although eight portions are shown in FIG. 7, the present invention is not limited to eight or any other specific multiple of data path widths. Once the wide operand portions 730A-H are sequentially loaded, they may be used as a single wide operand 735 by the functional element 740, which may be any element(s) from FIG. 1 connected thereto. The result of the wide operand is then provided to a result register 745, which in a presently preferred embodiment is of the same width as the memory width.

Detailed Description Text (26):
Referring next to FIG. 9, an exemplary arrangement of the data structures of the wide microcache or dedicated storage 114 may be better appreciated. The wide microcache contents, wmc.c, can be seen to form a plurality of data path widths 900A-n, although in the example shown the number is eight. The physical address, wmc.pa, is shown as 64 bits in the example shown, although the invention is not limited to a specific width.

The size of the contents, wmc.size, is also provided in a field which is shown as 10 bits in an exemplary embodiment. A "contents valid" flag, wmc.cv, of one bit is also included in the data structure, together with a two bit field for thread last used, or wmc.th. In addition, a six bit field for register last used, wmc.reg, is provided in an exemplary embodiment. Further, a one bit flag for register and thread valid, or wmc.rtv, may be provided.

CLAIMS:

1. In a system having a data path functional unit having a functional unit data path width, a first memory system having a first data path width, and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width, a method comprising:

copying a first memory operand portion from the first memory system to the second memory system, the first memory operand portion having the first data path width;

copying a second memory operand portion from the first memory system to the second memory system, the second memory operand portion having the first data path width and being catenated in the second memory system with the first memory operand portion, thereby forming catenated data; and

reading at least a portion of the catenated data which is greater in width than the first data path width.

2. The method of claim 1 further comprising specifying a memory specifier from which a plurality of data path widths of data can be read.

6. In a system having a data path functional unit having a functional unit data path width, a first memory system having a first data path width, and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width, a method comprising:

copying a first memory operand portion from the first memory system to the second memory system, the first memory operand portion having the first data path width;

copying a second memory operand portion from the first memory system to the second memory system, the second memory operand portion having the first data path width;

catenating the second memory operand portion in the second memory system with the first memory operand portion, thereby forming catenated data; and

reading at least a portion of the catenated data which is greater in width than the first data path width.

7. The method of claim 6 further comprising specifying a memory specifier from which a plurality of data path widths of data can be read.

11. In a system having a data path functional unit having a functional unit data path width, a first memory system having a first data path width, and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width, a system comprising:

a first copying module configured to copy a first memory operand portion from the first memory system to the second memory system, the first memory operand portion having the first data path width;

a second copying module configured to copy a second memory operand portion from the first memory system to the second memory system, the second memory operand portion having the first data path width and being catenated in the second memory system with the first memory operand portion, thereby forming catenated data; and

a reading module configured to read at least a portion of the catenated data which is greater in width than the first data path width.

12. In a system having a data path functional unit having a functional unit data path width, a first memory system having a first data path width, and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width, a system comprising:

a first copying module configured to copy a first memory operand portion from the first memory system to the second memory system, the first memory operand portion having the first data path width;

a second copying module configured to copy a second memory operand portion from the first memory system to the second memory system, the second memory operand portion having the first data path width;

a catenating module configured to catenate in the second memory system the second memory operand portion with the first memory operand portion, thereby forming catenated data; and

a reading module configured to read at least a portion of the catenated data which is greater in width than the first data path width.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 5. Document ID: US 6295299 B1

L5: Entry 5 of 18 File: USPT Sep 25, 2001

DOCUMENT-IDENTIFIER: US 6295299 B1
TITLE: Data path architecture for a LAN switch

CLAIMS:

7. The packet switch of claim 1, wherein the y-bit wide data path is twice the width of the multiple-bit wide data path.

8. In a packet switch, a method of receiving a data packet from a communications medium coupled thereto, comprising:

receiving the data packet at an interface coupled to the communications medium;

transmitting multiple bits of the data packet over a multiple-bit wide data path;

routing separate n-bit portions of the multiple bits via p n-bit wide data paths coupled to the multiple-bit wide data path, wherein n times p equals the width of the multiple bit wide data path;

buffering x bits at each n-bit wide data path, where x is a multiple of n; and

concurrently forwarding y bits from the p n-bit wide data paths, where y equals x times p.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 6. Document ID: US 6076173 A

L5: Entry 6 of 18 File: USPT Jun 13, 2000

DOCUMENT-IDENTIFIER: US 6076173 A
TITLE: Architectural coverage measure

CLAIMS:

1. A method for determining a coverage measure for selecting defect screening tests for a system having a control, data path and cache, said method comprising:

obtaining a coverage measure by determining the effective bit width for a plurality of data path blocks; and

using said coverage measure as a measure of system level coverage.

☐ 7. Document ID: US 5983296 A

L5: Entry 7 of 18 File: USPT Nov 9, 1999

DOCUMENT-IDENTIFIER: US 5983296 A
TITLE: Method and apparatus for terminating busses having different widths

CLAIMS:

1. In an apparatus comprising an adapter card and a plurality of interconnect cables coupled thereto, a method for automatically terminating at least one of the plurality of interconnect cables, comprising the steps of:

determining whether a first device having a first data path width is connected to at least one of the plurality of interconnect cables; and

determining whether a second device having a second data path width is connected to at least one of the plurality of interconnect cables; and

selectively coupling at least one terminator circuit on the adapter card to at least one of the interconnect cables.

7. In an apparatus comprising an adapter card and a plurality of connectors, at least two of the plurality of connectors having different numbers of electrical contacts, a method for automatically terminating an interconnect cable coupled to one of the plurality of connectors, comprising the steps of:

determining whether a device having a first data path width is connected to the interconnect cable;

selectively coupling at least one terminator circuit on the adapter card to the interconnect cable; and

a second interconnect cable coupled to another of the plurality of connectors, wherein the second interconnect cable is attached to a second device having a second data path width different than the first data path width.

8. A method for automatically terminating a data bus having a plurality of interconnect cables coupled to a controller, comprising the steps of:

sensing whether a first device having a first data path width is connected to any of the interconnect cables;

sensing whether a second device having a second data pat width different than the first data path width is connected to any of the interconnect cables;

selectively coupling at least one terminator circuit on the controller to the data bus.

☐ 8. Document ID: US 5926420 A

L5: Entry 8 of 18 File: USPT Jul 20, 1999

DOCUMENT-IDENTIFIER: US 5926420 A
TITLE: Merged Memory and Logic (MML) integrated circuits including data path width reducing circuits and methods

Detailed Description Text (5):
In order to reduce the number of data paths during test mode, at least one data path width reducing circuit 105 is provided. The data path width reducing circuit is responsive to a test mode signal, to serially provide output data on the first plurality of data paths 102 to at least one MML integrated circuit output pad 109, wherein the number of MML integrated circuit output pads is less than the first plurality, to thereby reduce an external data path width of the MML integrated circuit during test mode. The data path width reducing circuit may also serially provide input data from at least one MML integrated circuit input pad 113 to the second plurality of input data paths 104, wherein the number of MML integrated circuit input pads is less than the second plurality.

CLAIMS:

1. A merged memory and logic (MML) integrated circuit comprising:

a memory block;

a logic block;

a first plurality of output data paths that interconnect the memory block and the logic block for communication therebetween in a normal mode; and

a data path width reducing circuit that is separate from the logic block and that is responsive to a test mode signal, to serially provide output data on the first plurality of data paths to at least one MML integrated circuit output pad, wherein the number of MML integrated circuit output pads is less than the first plurality, to thereby reduce an external data path width of the MML integrated circuit during test mode.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

☐ 9. Document ID: US 5896395 A

L5: Entry 9 of 18 File: USPT Apr 20, 1999

DOCUMENT-IDENTIFIER: US 5896395 A
TITLE: Integrated circuit memory devices and operating methods including temporary data path width override

Abstract Text (1):

An integrated circuit memory device includes an array of memory cells having a selectable first or second data path width. The integrated circuit memory device also includes a circuit which permanently selects one of the first and second data path widths for permanent operation of the integrated circuit memory device, and which temporarily overrides the permanent selection, to thereby temporarily operate the integrated circuit memory device using the other data path width. Accordingly, for example, when the first path width is a 16 bit path width and the second path width is a 4 bit path width, the path width is permanently selected during manufacturing of the integrated circuit memory device, to thereby manufacture 16 bit path width or 4 bit path width devices. However, during testing, the 16 bit path width devices may be temporarily overridden and tested as 4 bit path width devices. The number of test pins which are required can therefore be reduced and testing efficiency can be improved.

Brief Summary Text (14):
In particular, integrated circuit memory devices according to the invention include an array of memory cells having a selectable one of first and second data path widths. A circuit is also included which permanently selects one of the first and second data path widths for permanent operation of the integrated circuit memory device. The circuit also temporarily overrides the permanent selection of the one of the first and second data path widths, to thereby temporarily operate the memory using the other of the first and second data path widths.

Brief Summary Text (15):
Preferably, the circuit is activated during manufacture of the integrated circuit memory device to permanently select one of the first and second data path widths for operation of the integrated circuit memory device. The circuit is also activated during testing of the integrated circuit memory device, to allow testing of the integrated circuit memory device using the other of the first and second data path widths.

Brief Summary Text (17):
The circuit which permanently selects and temporarily overrides may include a mode register, a first data path width selection signal generator and a second data path width selection signal generator. The mode register generates a mode control signal in response to an input signal. The input signal may be applied during testing. The first data path width selection signal generator is responsive to a permanent first data path selection signal, for example permanent application of power supply voltage, ground voltage or another voltage, to a first data path pad, to permanently select the first data path width. However, the first data path width selection signal generator is also responsive to the temporary override signal, to temporarily override selection of the first data path width.

Brief Summary Text (20):
An embodiment of the first data path width selection signal generator comprises a first integrated circuit bonding pad and a second transfer circuit which transfers a permanent first data path width selection signal which is received from the first bonding pad. A second logic circuit combines the transferred first bonding signal and the mode control signal to permanently select the first data path width in response to the permanent first data path width selection signal unless the mode control signal temporarily overrides the permanent first data path width selection signal.

Brief Summary Text (21):
Similarly, the second data path width selection signal generator includes a second integrated circuit bonding pad and a third transfer circuit which transfers a permanent second data path width selection signal which is received from the second bonding pad. A third logic circuit combines the transferred second bonding signal and the mode control signal to permanently select the second data path width in response to the permanent first data path width selection signal unless the mode control signal temporarily overrides the permanent second path width selection signal.

Brief Summary Text (23):
Accordingly, integrated circuit memory devices including an array of memory cells having a selectable one of first and second data path widths are operated, by permanently selecting one of the first and second data path widths for permanent operation of the integrated circuit memory device. The permanent selection is temporarily overridden, to thereby temporarily operate the memory using the other of the first and second data path widths. The permanently selecting step is preferably performed during manufacture of the integrated circuit memory device to permanently select one of the first and second data path widths for operation. The temporary overriding step is preferably performed during testing of the integrated circuit memory

device to test the integrated circuit memory device using the other of the first and second data path widths. Thus, testing efficiency may be increased by using fewer number of tester input/output pins.

Detailed Description Text (3):
Referring now to FIG. 2, a block diagram of integrated circuit memory devices according to the present invention is now illustrated. As shown in FIG. 2, an integrated circuit memory device 200 includes an array of memory cells 220. The memory cell array 220 can operate one of a selectable first and second data path width. The first data path width is selected by first data path selection signal x16. The second data path width is selected by a second data path signal x4. The selection of data path widths for memory cell arrays of integrated circuit memory devices are well known to those having skill in the art and will not be described further herein.

Detailed Description Text (4):
Still referring to FIG. 2, a first data path width selection signal generator, shown as x16 mode selection signal generator 240, is responsive to a permanent first data path selection signal x16.sub.-- PAD to generate the first data path selection signal x16. Similarly, the second data path selection signal generator, shown as x4 mode selection signal generator 260, is responsive to permanent selection of a second data path selection signal x4.sub.-- PAD, to generate second data path width selection signal x4. An embodiment of x16 mode selection signal generator 240 and x4 mode selection signal generator 260 will be described in connection with FIGS. 3 and 4 respectively.

CLAIMS:

1. An integrated circuit memory device comprising:

an array of memory cells having a selectable one of first and second data path widths, such that the memory device can operate as a selectable one of an m bit by n memory device and an m/x bit by nx memory device; wherein x is an integer and

a circuit which permanently selects one of the first and second data path widths for permanent operation of the integrated circuit memory device, such that the memory device permanently operates as one of an m bit by n memory device and an m/x bit by nx memory device, and which temporarily overrides the permanent selection of the one of the first and second data path widths, to thereby temporarily operate the memory using the other of the first and second data path widths, such that the memory device temporarily operates as the other of an m bit by n memory device and an m/x bit by nx memory device.

2. An integrated circuit memory device according to claim 1:

wherein the circuit is activated during manufacture of the integrated circuit memory device to permanently select one of the first and second data path widths for operation of the integrated circuit memory device; and

wherein the circuit is also activated during testing of the integrated circuit memory device to temporarily test the integrated circuit memory device using the other of the first and second data path widths.

5. An integrated circuit memory device according to claim 1 wherein the circuit comprises:

a mode register which generates a mode control signal in response to an input signal;

a first data path width selection signal generator, which is responsive to a permanent first data path selection signal, to permanently select the first data path width, and which is also responsive to the temporary override signal, to temporarily override selection of the first data path width; and

a second data path width selection signal generator, which is responsive to a permanent second data path selection signal, to permanently select the second data path width, and which is also responsive to the temporary override signal, to temporarily override selection of the second data path width.

7. An integrated circuit memory device according to claim 6 wherein the first data path width selection signal generator comprises:

a first integrated circuit bonding pad;

a second transfer circuit which transfers a permanent first data path width selection signal which is received from the first bonding pad; and

a second logic circuit which combines the transferred first bonding signal and the mode control signal to permanently select the first data path width in response to the permanent first data path width selection signal unless the mode control signal temporarily overrides the permanent first data path width selection signal.

8. An integrated circuit memory device according to claim 7 wherein the second data path width selection signal generator comprises:

a second integrated circuit bonding pad;

a third transfer circuit which transfers a permanent second data path width selection signal which is received from the second bonding pad; and

a third logic circuit which combines the transferred second bonding signal and the mode control signal to permanently select the second data path width in response to the permanent first data path width selection signal unless the mode control signal temporarily overrides the permanent second data path width selection signal.

11. A method of operating an integrated circuit memory device including an array of memory cells having a selectable one of first and second data path widths, such that the memory device can operate as a selectable one of an m bit by n memory device and an m/x bit by nx memory device, wherein x is an integer the method comprising the steps of:

permanently selecting one of the first and second data path widths for permanent operation of the integrated circuit memory device, such that the memory device permanently operates as one of an m bit by n memory device and an m/x bit by nx memory device; and

temporarily overriding the permanent selection of the one of the first and second data path widths, to thereby temporarily operate the memory using the other of the first and second data path widths, such that the memory device temporarily operates as the other of an m bit by n memory device and an m/x bit by nx memory device.

12. A method according to claim 11:

wherein the step of permanently selecting is performed during manufacture of the integrated circuit memory device to permanently select one of the first and second data path widths for operation of the integrated circuit memory device; and

wherein the step of temporarily overriding is performed during testing of the integrated circuit memory device to temporarily test the integrated circuit memory device using the other of the first and second data path widths.

13. A method according to claim 11:

wherein the first data path width is a sixteen bit path width and the second data path width is a four bit path width;

wherein the step of permanently selecting is performed during manufacture of the integrated circuit memory device to permanently select a sixteen bit path width for operation of the integrated circuit memory device; and

wherein the step of temporarily overriding is performed during testing of the integrated circuit memory device to test the integrated circuit memory device using a four bit path width.

14. An integrated circuit memory device comprising:

an array of memory cells having a selectable one of first and second data path widths, such that the memory device can operate as a selectable one of an m bit by n memory device and an m/x bit by nx memory device; wherein x is an integer

a mode register, which is responsive to an input signal and a control signal, to

produce a mode control signal;

a first data path width mode selection signal generator, which is responsive to the mode control signal and to a first signal which is permanently applied thereto, and which selects the first data path width for the array of memory cells in response to the first signal, as long as the mode control signal is not produced by the mode register, such that the memory device permanently operates as one of an m bit by n memory device and an m/x bit by nx memory device; and

a second data path width mode selection signal generator, which is responsive to the mode control signal and to a second signal which is permanently applied thereto, and which selects the second data path width for the array of memory cells in response to the second signal, as long as the mode control signal is not produced by the mode register, such that the memory device temporarily operates as the other of an m bit by n memory device and an m/x bit by nx memory device.

15. An integrated circuit memory device according to claim 14 wherein the second data path width mode selection signal generator is also responsive to selection of the first data path width by the first data path width mode selection signal generator, to prevent the second data path width mode selection signal generator from selecting the second data path width for the memory cell array.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 10. Document ID: US 5881254 A

L5: Entry 10 of 18 File: USPT Mar 9, 1999

DOCUMENT-IDENTIFIER: US 5881254 A
TITLE: Inter-bus bridge circuit with integrated memory port

CLAIMS:

4. The bridge of claim 2 wherein said shared memory port has a data path width which is an integral multiple of a data path width of said secondary bus port and wherein said FIFO includes:

a plurality of FIFO elements where the number of said plurality of FIFO elements is equal the ratio of the said data path width of said shared memory port over said data path width of said secondary bus port.

12. The bridge of claim 10 wherein said shared memory port means has a data path width which is an integral multiple of a data path width of said secondary PCI bus port means and wherein said FIFO means includes:

a plurality of FIFO elements where the number of said plurality of FIFO elements is equal the ratio of the said data path width of said shared memory port means over said data path width of said secondary PCI bus port means.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

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☐ 11. Document ID: US 5815437 A

L5: Entry 11 of 18 File: USPT Sep 29, 1998

DOCUMENT-IDENTIFIER: US 5815437 A
TITLE: Data input/output managing device, particularly for a non-volatile memory

CLAIMS:

17. The data input/output managing apparatus of claim 16, further comprising an input to receive a word length signal, and wherein the first, second and third data paths are parallel data paths having a width equal to a number of bits, and wherein the width of each of the first, second and third data paths is set by the apparatus in response to the word length signal.

20. The data input/output managing apparatus of claim 14, further comprising an input to receive a word length signal, and wherein the first and second data paths are parallel data paths having a width equal to a number of bits, and wherein the width of each of the first and second data paths is set by the apparatus in response to the word length signal.

26. The method of claim 25, wherein each of the first, second and third data paths are parallel data paths having a width equal to a number of bits, the method further comprising a steps of:

receiving a control signal; and

setting the width of the first, second and third data paths based on a state of the control signal.

28. The method of claim 22, wherein each of the first and second data paths are parallel data paths having a width equal to a number of bits, the method further comprising steps of:

receiving a control signal; and

setting the width of the first and second data paths based on a state of the control signal.

34. The data input/output managing apparatus of claim 32, wherein the first, second and third data paths are parallel data paths having a width equal to a number of bits, the data input/output apparatus further comprising means for setting the width of each of the first, second and third data paths.

36. The data input/output managing apparatus of claim 29, wherein the first and second data paths are parallel data paths having a width equal to a number of bits, the data input/output apparatus further comprising means for setting the width of each of the first and second data paths.

☐ 12. Document ID: US 5745791 A

L5: Entry 12 of 18 File: USPT Apr 28, 1998

DOCUMENT-IDENTIFIER: US 5745791 A
TITLE: System for interfacing first and second components having different data path width by generating first and second component address to read data into buffer

CLAIMS:

10. A method for interfacing a memory with a bus of a computer system having a data path width different from that of the memory, comprising the steps of:

(A) coupling an input of a first buffer to the memory and an output of the first buffer to the bus, wherein the first buffer has an input data path width equal to the data path width of the memory and an output data path width equal to the data path width of the bus, wherein the input data path width of the first buffer is not equal to the output data path width of the first buffer;

(B) coupling an input of a second buffer to the bus and an output of the second buffer to the memory, wherein the second buffer has an output data path width equal to the data path width of the memory and an input data path width equal to the data path width of the bus, wherein the input data path width of the second buffer is not equal to the output data path width of the second buffer; and

(C) generating (1) a first and a second memory address in accordance with a first address and (2) a third and a fourth memory address in accordance with a second address from the bus, wherein the first and second memory addresses cause first and second portions of a first data to be sequentially read from the memory into the first buffer, wherein the third and fourth memory addresses cause first and second portions of a second data to be sequentially written into the memory from the second buffer.

13. An apparatus for interfacing a first component with a second component having a data path width different from that of the first component, comprising:

(A) a first buffer coupled to the first and second components and having an input data path width equal to the data path width of the first component and an output data path width equal to the data path width of the second component, wherein the input data path width of the first buffer is not equal to the output data path width of the first buffer; and

(B) an address generation circuit coupled to the first and second components, wherein the address generation circuit receives a first address from the second component and generates a first and a second component address to cause a first and a second portion of a first data to be read from the first component into the first buffer.

14. The apparatus of claim 13, further comprising a second buffer coupled to the first and second components and having an output data path width equal to the data path width of the first component and an input data path width equal to the data path width of the second component, wherein the input data path width of the second buffer is not equal to the output data path width of the second buffer.

20. An apparatus for interfacing a first component with a second component having a data path width different from that of the first component, comprising:

(A) a first buffer coupled to the first and second components and having an input data path width equal to the data path width of the first component and an output data path width equal to the data path width of the second component, wherein the input data path width of the first buffer is not equal to the output data path width of the first buffer; and

(B) an address generation circuit coupled to the first and second components, wherein the address generation circuit receives a first address from the second component and generates a first and a second component address to cause a first and a second portion of a first data to be written into the first component from the first buffer.

21. The apparatus of claim 20, further comprising a second buffer coupled to the first and second components and having an output data path width equal to the data path width of the first component and an input data path width equal to the data path width of the second component, wherein the input data path width of the second buffer is not equal to the output data path width of the second buffer.

27. An apparatus for interfacing a first component with a second component having a data path width different from that of the first component, comprising:

(A) a first buffer coupled to the first and second components and having an input data path width equal to the data path width of the first component and an output data path width equal to the data path width of the second component, wherein the first buffer stores a first and a second portion of a first data, wherein the input data path width of the first buffer is not equal to the output data path width of the first buffer;

(B) a second buffer coupled to the first and second components and having an output

data path width equal to the data path width of the first component and an input data path width equal to the data path width of the second component, wherein the second buffer stores a first and a second portion of a second data, wherein the input data path width of the second buffer is not equal to the output data path width of the second buffer; and

(C) an address generation circuit coupled to the first and second components, wherein the address generation circuit receives a first and a second address from the second component and generates (1) a first and a second component address from the first address to cause the respective first and second portions of the first data to be sequentially read from the first component and (2) a third and a fourth component address from the second address to cause the respective first and second portions of the second data to be sequentially written into the first component.

☐ 13. Document ID: US 5721841 A

L5: Entry 13 of 18 File: USPT Feb 24, 1998

DOCUMENT-IDENTIFIER: US 5721841 A
TITLE: Adapter having data aligner including register being loaded to or from memory with an offset in accordance with predetermined network fragmentation parameters

CLAIMS:

10. A data aligner for transferring data from a first data path having a width of M bits to a second data path having a width of N bits, where N is larger than M, while aligning the data at any selected byte boundary at the second path, comprising:

a register arrangement comprising a first M bit register, a second M bit register, and a third M bit register, arranged such that data can be shifted from said third register to said second register, and from said second register to said first register in response to a shift command;

means for loading data from said first path into said third register and for selectably offsetting said data by a selectable number of bytes in the direction of said first register;

means for shifting said data in the direction of said first register by M bits; and

means for reading said data from said register arrangement to said second path.

13. A data aligner for transferring data from a first data path having a width of 32 bits to a second data path having a width of 64 bits, while aligning the data at any selected byte boundary at the second path, comprising:

a register arrangement comprising a first thirty-two bit register, a second thirty-two bit register, and a third thirty-two bit register, arranged such that data can be shifted from said third register to said second register, and from said second register to said first register;

means for loading data from said first path into said third register and for selectably offsetting said data by zero, one, two or three bytes in the direction of said first register;

means for shifting said data in the direction of said first register by thirty-two bits; and

means for reading said data from said register arrangement to said second path.

☐ 14. Document ID: US 5515507 A

L5: Entry 14 of 18 File: USPT May 7, 1996

DOCUMENT-IDENTIFIER: US 5515507 A
TITLE: Multiple width data bus for a microsequencer bus controller system

Brief Summary Text (12):
There have been various attempts to provide a multiple or variable width data path. In Matick, et. al., U.S. Pat. No. 4,663,729, and Dill, et. al., U.S. Pat. No. 4,667,305, is disclosed a display architecture which supports data path widths of 32, 64, 128, and 256 bits. However, the disclosed system does not provide for extensive parity generation and checking as does the present invention, nor does it support 36-bit data words. A data bus being operable with 8-bit, 16-bit or 32-bit modes is shown in Kinoshita, U.S. Pat. No. 5,113,369. The data bus shown is used in a computer system capable of executing programs containing instructions and data consisting of 16-bit or 32-bit words. This system does not show the use of 32-bit and 36-bit data words or parity generation logic. A dual bit length protocol is described in Frank, U.S. Pat. No. 5,255,376, which is capable of transferring data in 32-bit or 64-bit words. The Frank system is designed to transfer data in one of two word sizes, but the size of one must be twice the size of the other (i.e., 32 and 64). In addition, no parity error detection logic is described. What the prior an is lacking is a bus with associated parity generation and parity checking logic which will transfer either 32-bit or 36-bit data words without using duplicate signal lines.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

☐ 15. Document ID: US 5506992 A

L5: Entry 15 of 18 File: USPT Apr 9, 1996

DOCUMENT-IDENTIFIER: US 5506992 A
TITLE: Distributed processing system with asynchronous communication between processing modules

Detailed Description Text (7):
FIG. 5 shows how the individual ALUs 19 of set 2 are cascade connected with each other on an individual chip 1, and how the ALU cascades 2 of adjacent parallel chips 1 are interconnected to propagate Arithmetic Carry 16 and Right/Left Shift signals to form multiple-width data paths, as determined by the values stored in each respective chip's 1 Global Control Registers 3. Each ALU 19 of set 2 consists of a cascade of Logical 22, Arithmetic 23, and Shift 24 sections. Each ALU set 2 also contains Input Registers 25 and Output Registers 26.

Detailed Description Text (9):
FIG. 7 gives an example of the calculation of the polynomial AX.sup.3 +BX.sup.2 +CX+D by utilizing some 24 chips 1, with the restriction that chips 1 spanning multiple width segments of the data path must be horizontally adjacent for interconnection of intervening Carry and Shift signals.

☐ 16. Document ID: US 5388240 A

L5: Entry 16 of 18 File: USPT Feb 7, 1995

DOCUMENT-IDENTIFIER: US 5388240 A
TITLE: DRAM chip and decoding arrangement and method for cache fills

Brief Summary Text (7):
a) the line length L is a multiple of the data path width W

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments KWIC | Draw Desc | Image

☐ 17. Document ID: US 5168562 A

L5: Entry 17 of 18 File: USPT Dec 1, 1992

DOCUMENT-IDENTIFIER: US 5168562 A
**** See image for Certificate of Correction ****
TITLE: Method and apparatus for determining the allowable data path width of a device in a computer system to avoid interference with other devices

CLAIMS:

1. An apparatus for setting the operating data path width of a unit which can operate in a predetermined portion of an address space on either of a first data path width or a second, wider data path width, responds based on a decode of a first series of address lines when operating on the first data path width and responds based on a decode of a second series of address lines when operating on the second data path width, the second series of address lines have a minimum portion decode size of the size of the predetermined portion of the address space in which the unit operates, and the first series of address lines having a minimum decode size of the first data path width, the unit connected to a computer system at a particular location, the computer system having a first data path of the first data path width and a second data path having a width equal to the second data path width less the first data path width, the second data path combining with the first data path to allow use of the second data path width, having one ground connection associated with the second data path to allow determination of the presence of the second data path at each connection location and having locations for connection of a plurality of devices operating in the predetermined portion of the address space, the plurality of devices including units operating on the first data path width and units operating on the second data path width, the apparatus comprising:

means for operating the unit at the first data path width when a bit is set to a first state and at the second data path width when said bit is set to a second state;

means for determining if only the first data path width is available to the unit by monitoring the presence of said one ground connection associated with said second data path; and

means coupled to said means for operating the unit and said means for determining if only the first data path width is available and responsive to said means for determining if only the first data path width is available determining the availability of only the first data path width for setting said bit of said means for operating the unit to said first state.

2. The apparatus of claim 1, further comprising:

means for determining if devices operating on the second data path width are present in the predetermined portion of the address space; and

means coupled to said means for operating the unit, said means for determining if only the first data path width is available and said means for determining if devices on the second data path width are present and responsive to said means for determining if only the first data path width is available determining the availability of the second data path width and responsive to said means for determining if devices on the second data path width are present determining the presence of second data path width operating devices for setting said bit of said means for operating the unit to said second state.

3. The apparatus of claim 2, further comprising:

means for determining if devices operating on the first data path width are present in the predetermined portion of the address space; and

means coupled to said means for operating the unit, said means for determining if only the first data path width is available, said means for determining if devices operating on the first data path width are present and said means for determining if devices operating on the second data path width are present and responsive to said means for determining if only the first data path width is available determining the availability of the second data path width, responsive to said means for determining if devices on the second data path width are present determining the lack of devices and responsive to said means for determining if devices operating on the first data path width are present determining the presence of devices for setting said bit of said means for operating the unit to said first state.

4. The apparatus of claim 3, further comprising:

means said means for determining if only the first data path width is available and said means for determining if devices on the second data path width are present and responsive to said means for determining if only the first data path width is available determining the availability of only the first data path width and responsive to said means for determining if devices on the second data path width are present determining the presence of devices for providing a warning indication to the operator of the computer system.

5. The apparatus of claim 3, further comprising:

means coupled to said means for operating the unit, said means for determining if devices operating on the first data path width are present and said means for determining if devices on the second data path width are present and responsive to said means for determining if devices operating on the first data path width are present determining the lack of devices and responsive to said means for determining if devices on the second data path width are available determining the lack of devices for setting said bit of said means for operating the unit to said first state.

6. The apparatus of claim 3, wherein said means for determining if devices operating on the first data path width are present includes:

means coupled to said means for operating the unit for setting said bit of said means for operating the unit to said second state;

means for writing a value to each of a series of locations in the predetermined portion of the address space;

means for reading a value from each of said series of locations in the predetermined portion of the address space after writing to each of said series of locations in the predetermined portion of the address space;

means coupled to said means for writing a value and to said means for reading a value for determining if the read value is equal to the written value and determining that a device operating on the first data path width is present if equal;

means coupled to said means for determining if the read value is equal to the written value for reading a value at each of said series of locations and determining if said

second read value is equal to a predetermined value for each of said series of locations in the predetermined address space where said means for determining if the read value is equal to the written value does not determine that a device operating on the first data width is present;

means coupled to said means for determining if the second read value is equal to the predetermined value for reading a second data path width value rom each of said series of locations in the predetermined address space where said means for determining if the read value is equal to the predetermined value determines the values are equal; and

means coupled to said means for reading a second data path width value from each of said series of locations for determining if said read second path width value is equal to a predetermined value and determining that a device operating on the first data path width is present if not equal.

8. The apparatus of claim 7, further comprising:

means coupled to said means for operating the unit, said means for indicating a desired operating data path width and said means for setting said bit of said means for operating the unit to said second state and responsive to said means for indicating a desired operating data path width indicating operation on the first data path width for setting said bit of said means for operating the unit to said first state and for overriding said means for setting said bit of said means for operating the unit to said second state.

9. The apparatus of claim 8, further comprising:

means for determining if devices operating on the second data path width are present in the predetermined portion of the address space; and

means coupled to said means for indicating a desired operating data path width, said means for determining if devices operating on the second data path width are present and said means for means for determining if only the first data path width is available and responsive to said means for determining if only the first data path width is available determining the availability of the second data path width, responsive to said means for determining if devices operating on the second data path width are present determining the presence of devices and responsive to said means for indicating a desired operating path width indicating operation on the first data path width for providing a warning indication to the operator of the computer system.

11. The apparatus of claim 7, further comprising:

means coupled to said means for indicating a desired operating data path width and said means for means determining if only the first data path width is available and responsive to said means for indicating a desired data width indicating second width operation and responsive to said means for determining if only the first data path width is available indicating the availability of only the first data path width for providing a warning indication to the operator of the computer system.

12. The apparatus of claim 7, further comprising:

means coupled to said means for indicating a desired operating data path width, said means for operating the unit and said means for determining if only the first data path width is available and responsive to said means for indicating a desired data path width indicating the second data path width and responsive to said means for determining if only the first data path width is available indicating the availability of the second data path for setting said bit of said means for operating the unit to said second state.

13. The apparatus of claim 12, further comprising:

means for determining if devices operating on the first data path width are present in the predetermined portion of the address space; and

means coupled to said means for indicating a desired operating data path width, said means for determining if devices operating on the first data path width are present in the second address space and said means for means for determining if only the first data path width is available and responsive to said means for indicating a desired operating data path width means indicating the second data path width, responsive to

said means for determining if only the first data path width is available determining the availability of the second data path width and responsive to said means for determining if devices operating on the first data path width are present determining the presence of devices for providing a warning message to the operator of the computer system.

15. A machine implemented method for setting the operating data path width of a unit which can operate in a predetermined portion of an address space on either of a first data path width or a second, wider data path width , responds based on a decode of a first series of address lines when operating on the first data path width and responds based on a decode of a second series of larger address lines when operating on the second data path width, the second series of address liens having a minimum portion decode size of the size of the predetermined portion of the address space in which the unit operates, the first series of address lines having a minimum decode size of the first data path width and having a means for operating the unit at the first data path width when a bit is set to a first state and at the second data path width when said bit is set to a second state, the unit connected to a computer system at a particular location computer system having a first data path of the first, narrow data path width and a second data path having a width equal to the second, wider data path width less the first data path width, the second data path combining with the first data path to allow use of the second data path width, having one ground connection associated with the second data path to allow determination of the presence of the second data path at each connection location and having locations for connection of a plurality of devices operating in the predetermined portion of the address space, the plurality of devices including units operating on the first data path width and units operating on the second data path width, the machine implemented method comprising:

determining if only the first data path width is available to the unit by monitoring the presence of said one ground connection associated with said second data path; and

setting said bit of the means for operating the unit to said first state responsive to determining the availability of only the first data path width.

17. The machine implemented method of claim 13, further comprising:

determining if devices operating on the first data path width are present in the predetermined portion of the address space; and

setting said bit of the means for operating the unit to said first state responsive to determining the availability of the second data path width, responsive to determining the lack of second data path width devices and responsive to determining the presence of first data path width devices.

18. The machine implemented method of claim 17, further comprising:

providing a warning indication to the operator of the computer system responsive to determining the availability of only the first data path width and responsive to determining the presence of second data path width devices.

19. The machine implemented method of claim 14, further comprising:

setting said bit of the means for operating the unit to said first state responsive to determining the lack of first data path width devices and responsive to determining the lack of second data width path devices.

20. The machine implemented method of claim 14, wherein said step of determining if devices operating on the first data path width are present includes:

setting said bit of the means for operating the unit to said second state;

writing a value to each of a series of locations in the predetermined portion of the address space;

reading a first value from each of said series of locations in the predetermined portion of the address space after writing to each of said series of locations in the predetermined portion of the address space;

determining if the first read value is equal to the written value and determining that a device operating on the first data path width is present if equal;

reading a second value from each of said series of locations and determining if said second read value is equal to a predetermined value for each of said series of locations in the predetermined address space after determining that the first read value and the written value are not equal;

reading a second data path width value from each of said series of locations in the predetermined address space where the read value and the predetermined value and equal; and

determining if said read second data path width value is equal to a predetermined value and determining that a device operating on the first data path width is present if not equal.

23. The machine implemented method of claim 17 further comprising:

setting said bit of the means for operating the unit to said first state and overriding setting said operating means bit to said second state responsive to indicating operation on the first data path width.

24. The machine implemented method of claim 23, further comprising:

determining if devices operating on the second data path width are present in the predetermined portion of the address space; and

providing a warning indication to the operator of the computer system responsive to determining the availability of the second data path width, responsive to determining the presence of second data path width devices and responsive to indicating operation on the first data path width.

26. The machine implemented method of claim 17, further comprising:

providing a warning indication to the operator of the computer system responsive to indicating second width operation and responsive to determining the availability of only the first data path width.

28. The machine implemented method of claim 27, further comprising:

determining if devices operating on the first data path width are present in the predetermined portion of the address space; and

providing a warning message to the operator of the computer system responsive to indicating the second data path width, responsive to determining the availability of the second data path width and responsive to determining the presence of second data path width devices.

☐ 18. Document ID: US 4965723 A

L5: Entry 18 of 18 File: USPT Oct 23, 1990

DOCUMENT-IDENTIFIER: US 4965723 A
TITLE: Bus data path control scheme

Brief Summary Text (11):
The bus data path controller controls a system that includes a plurality of buses, where each bus has a data path width equal to or greater than a data path width of a subsystem having the greatest data path width. The subsystems that have different data path widths may be coupled to each of the buses. The bus data path controller controls the flow of data between subsystems over the buses.

CLAIMS:

1. A data path controller in a data processing system that includes a central processor unit and a plurality of subsystems, the controller providing for a transfer of data between subsystems having different data path widths, comprising:

a plurality of buses intercoupling the central processing unit and the plurality of subsystems, each bus having a data path width equal to or greater than a data path width of a subsystem having the greatest data path width, wherein at least two subsystems having differing data path widths are coupled to the same one of said plurality of buses; and

means for controlling a flow of data between subsystems over said plurality of buses, said means for controlling being coupled to said plurality of buses and comprising,

means for producing a control signal in response to a request to transfer data from a sending subsystem, which is coupled to one of the plurality of buses, to a receiving subsystem, which is coupled to one of the plurality of buses, and

means for controlling the data width of a flow of data between any two of said plurality of buses, said means for controlling the data width being responsive to said control signal so that data from said sending subsystem is transferred to said receiving subsystem, wherein said means for controlling the data width is coupled between any two of said plurality of buses and receiving the control signal from said means for producing a control signal.

5. A data path controller in a data processing system that includes a central processor unit and a plurality of subsystems, the controller providing for a transfer of data between subsystems having different data path widths, comprising:

a plurality of buses intercoupling the central processing unit and the plurality of subsystems, each bus having a data path width equal to or greater than a data path width of a subsystem having the greatest data path width, wherein at least two subsystems having differing data path widths are coupled to the same one of said plurality of buses; and

means for controlling a flow of data between subsystems over said plurality of buses, said means for controlling being coupled to said plurality of buses and comprising,

means for producing a control signal in response to a request to transfer data from a sending subsystem, which is coupled to one of the plurality of buses, to a receiving subsystem, wherein said means for producing the control signal comprises a control logic circuit, and

means for controlling the data width of a flow of data between any two of said plurality of buses, said means for controlling the data width being responsive to said control signal so that data from said sending subsystem is transferred to said receiving subsystem, wherein said means for controlling the data width of a flow of data comprises means for converting the data width of the data from said sending subsystem to the data width associated with said receiving subsystem, said means for controlling the data width is coupled between any two of said plurality of buses and receiving the control signal from said means for producing a control signal.

Terms	Documents
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Mackly Monestime

L1	1492	S	(PLURALITY OR MULTIPLE OR MORE THAN ONE) (3A) DATA PATH
L2	749	S	(PLURALITY OR MULTIPLE OR MORE THAN ONE) (3A) DATA (2A) WIDT
L3	118001	S	(PLURALITY OR MULTIPLE OR MORE THAN ONE OR FIRST) (3A) MEMOR
L4	33	S	L1 (P) L2
L5	3	S	L4 (P) L3
L6	15387	S	FIRST MEMORY (P) SECOND MEMORY
L7	0	S	L4 (P) L6
L8	3	S	L4 AND L6
L9	2196	S	L1 OR L2
L10	203	S	L3 (P) L9
L11	0	S	L10 (P) CATENAT? (3A) DATA
L12	1	S	L10 AND CATENAT? (3A) DATA

Mackly Monestime

L5 ANSWER 1 OF 3 USPATFULL
PI US 6295599 B1 20010925
DETD The wide function unit may be better appreciated from FIG. 7, in which a register number 700 is provided to an operand checker 705. Wide operand specifier 710 communicates with the operand checker 705 and also addresses memory 715 having a defined memory width. The **memory** address includes a **plurality** of register operands 720A-n, which are accumulated in a dedicated storage portion 714 of a data functional unit 725. In the exemplary embodiment shown in FIG. 7, the dedicated storage 714 can be seen to have a width equal to eight data path widths, such that eight wide operand portions 730A-H are sequentially loaded into the dedicated storage to form the wide operand. Although eight portions are shown in FIG. 7, the present invention is not limited to eight or any other specific **multiple** of **data path widths**. Once the wide operand portions 730A-H are sequentially loaded, they may be used as a single wide operand 735 by the functional element 740, which may be any element(s) from FIG. 1 connected thereto. The result of the wide operand is then provided to a result register 745, which in a presently preferred embodiment is of the same width as the memory width.

L5 ANSWER 2 OF 3 USPATFULL
PI US 5831890 19981103
CLM What is claimed is:
19. A single in-line memory module for memory expansion in a computer system having a memory bus and an input for receiving a first reference voltage, said single in-line memory module comprising the elements of: a printed circuit board, said printed circuit board having a first side and a second side, said printed circuit board having an electrical connector, said electrical connector including a first set of electrical contacts on said first side of said printed circuit board and a second set of electrical contacts on said second side of said printed circuit board; a **first** set of **memory** elements arranged on said printed circuit board, said **first** set of **memory** elements having a total of at least n data lines; a driver circuit mounted on said printed circuit board, said driver circuit coupled to a set of control signals in said electrical connector, said driver circuit transmitting said control signals to said **first** set of **memory** elements; wherein said memory elements and said driver circuit operate at a second reference voltage; and a voltage regulation circuit, mounted on said printed circuit board and coupled to at least **one memory** element of said **first** set of **memory** elements and said driver circuit, said voltage regulation circuit converting the first reference voltage into the second reference voltage and providing the second reference voltage to the memory elements and the driver circuit; wherein said electrical connector includes a full **width data path** such that **one** of said single in-line memory modules increases a main memory in said computer system.

L5 ANSWER 3 OF 3 USPATFULL
PI US 5532954 19960702
CLM What is claimed is:
22. A single in-line memory module for memory expansion in a computer system having a memory bus with n data lines, said single in-line memory module comprising the elements of: a printed circuit board, said printed circuit board having a first side and a second side, said printed circuit board having an electrical connector, said electrical connector comprising a first set of electrical contacts on said first side of said

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printed circuit board and a second set of electrical contacts on said second side of said printed circuit board; a **first** set of **memory** elements arranged on said printed circuit board, said set of memory elements having a total of at least n data lines; and a driver circuit mounted on said printed circuit board, said driver circuit coupled to a set of control signals in said electrical connector, said driver circuit transmitting said controls signals to said **first** set of **memory** elements where in said electrical connector includes a full **width data path** such that **one** of said single in-line memory modules can increase a main memory in said computer system.

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